Preliminary

PALCE20V8H-15/25

EE CMOS Versatile Programmable Array Logic

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Pin, function and fuse-map compatible with all 24-pin GAL® devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High speed CMOS technology**
  - –15 ns propagation delay for "–15" version
  - –25 ns propagation delay for "–25" version
- **Direct plug-in replacement for a wide range of 24-pin PAL devices**
- **Outputs individually programmable as registered or combinatorial**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power-up**
- **Cost-effective 24-pin plastic DIP and PLCC packages**
- **Programmable on standard PAL device programmers**
- **Supported by PALASM® software**
- **Fully tested for high programming and functional yields and high reliability**

GENERAL DESCRIPTION

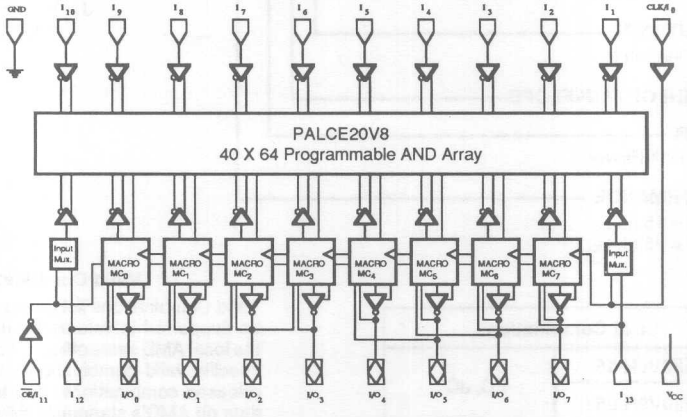
The PALCE20V8 is an advanced PAL® device built with low-power, high-speed, electrically-erasable CMOS technology. Its macrocells provide a universal device architecture. The PALCE20V8 is fully compatible with the GAL20V8 and can directly replace PAL20R8 series devices and most 24-pin combinatorial PAL devices.

Device logic is automatically configured according to the user's design specification. Design is simplified by PALASM design software, allowing automatic creation of a programming file based on Boolean or state equations. PALASM software also verifies the design and can provide test vectors for the finished device. Programming can be accomplished on standard PAL device programmers.

The PALCE20V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-HIGH or active-LOW output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

BLOCK DIAGRAM



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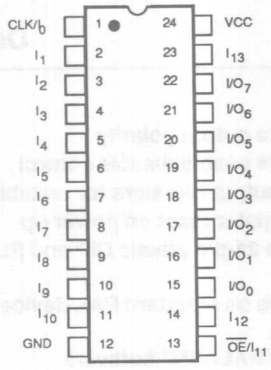
CONNECTION DIAGRAMS

SKINNYDIP



Pin Designations
I = IInput
I/O = Input/Output
CLK = Clock
VCC = Supply Voltage
GND = Ground

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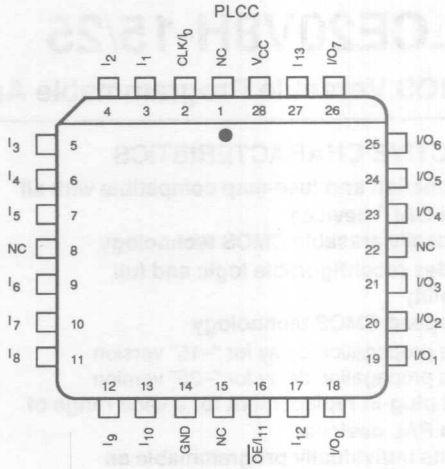
PLCC



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ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed/Power Option
c. Package Type
d. Operating Conditions

PAL CE 20 V 8 H -15 P C

a. PROGRAMMABLE ARRAY LOGIC

CMOS ELECTRICALLY ERASABLE

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF FLIP-FLOPS

b. POWER
H = Half Power

PERFORMANCE
–15 = 15 ns t_{PD}
–25 = 25 ns t_{PD}

d. OPERATING CONDITIONS
C = Commercial (0°C to +75°C)

c. PACKAGE TYPE
P = Plastic DIP, (PD 3024)
J = Plastic Leaded Chip Carrier, (PL 028)

Valid Combinations	
PALCE20V8H-15	PC, JC
PALCE20V8H-25	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Symbol	Type	Function
V_{CC}		Five Volt Power Input.
GND		Ground
CLK/I_0	TTL level Clock/input	If the CLK function is not used, it can used as a TTL input signal
$\overline{OE}/I_{11}$	TTL level Input	Output Enable. If the $\overline{OE}$ function is not used, it can be used as a TTL input signal.
$I_1..I_{10}, I_{12}, I_{13}$	TTL level inputs	Inputs 1 through 10 and Inputs 12 and 13
$I/O_0..I/O_7$	TTL level I/O	I/O_0 through I/O_7

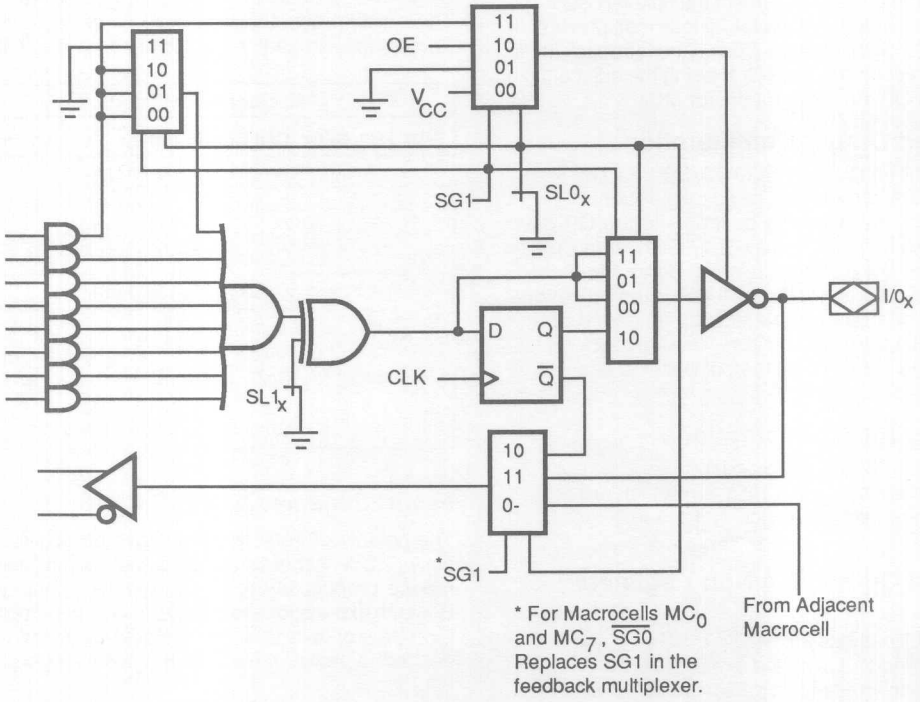
FUNCTIONAL DESCRIPTION

The PALCE20V8 is a universal PAL device. It has eight independently configurable macrocells ($MC_0..MC_7$). Each macrocell can be configured as a registered output, combinatorial output, combinatorial I/O, or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 13 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$) for all flip-flops.

Unused input pins should be tied directly to V_{CC} or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE20V8 are automatically configured from the user's design specification, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE20V8. First, it can be programmed as an emulated PAL device. This includes the PAL20R8 series and most combinatorial PAL devices. The PAL device programmer manufacturer will supply device codes for the standard PAL architectures to be used with the PALCE20V8. The programmer will program the PALCE20V8 to the corresponding PAL device architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed directly as a PALCE20V8. Here the user must use the PALCE20V8 device code. This option provides full utilization of the macrocells, allowing non-standard architectures to be built.



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PALCE20V8 Macrocell

Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, the buffer is always disabled. With the exception of MC_0 and MC_7, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. MC_0 derives its input from pin 13 ($\overline{OE}$) and MC_7 from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE20V8 will emulate a PAL20R8 family or a combinatorial device. Within each macrocell, SL0x, in conjunction with SG1, selects the configuration of the macrocell and $SL1_x$ sets the output as either active LOW or active HIGH.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In MC_0 and MC_7, SG0 replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for MC_7 and $\overline{OE}$ the adjacent pin for MC_0.

Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. $SL1_x$ is an input to the exclusive-OR gate which is the D input to the flip-flop. SL1x is programmed as 1 for inverted output or 0 for non-inverted output. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from Q on the register. The output buffer is enabled by $\overline{OE}$.

Combinatorial Configurations

The PALCE20V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

Dedicated Output in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Because the macrocell is a dedicated output, the feedback is not used. Because CLK and OE are not used in a non-registered device, pins 1 and 13 are available as input signals. Pin 1 will use the feedback path of MC_7 and pin 13 will use the feedback path of MC_0.

Dedicated Input in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for MC_0 and MC_7, the feedback signal is an adjacent I/O pin. For MC_0 and MC_7 the feedback signals are pins 1 and 13. These configurations are summarized in table 1 and illustrated in figure 2.

Combinatorial I/O in a Non-Registered Device

The control settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and OE are not used in a non-registered device, pins 1 and 13 are available as inputs. Pin 1 will use the feedback path of MC_7 and pin 13 will use the feedback path of MC_0.

Combinatorial I/O in a Registered Device

The control bit settings are SG0=0,SG1=1 and $SL0_x$ =1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

Macrocell Configuration				
SG0	**SG1**	**SL0x**	**Cell Configuration**	**Devices Emulated**
Device has registers				
0	1	0	Registered Output	PAL20R8, 20R6, 20R4
0	1	1	Combinatorial I/O	PAL20R6, 20R4
Device has no registers				
1	0	0	Combinatorial Output	PAL20L8, 20L2, 18L4,16L6,14L8
1	0	1	Dedicated Input	PAL20L2,18L4, 16L6
1	1	1	Combinatorial I/O	PAL20L8

Programmable Output Polarity

The polarity of each macrocell can be active HIGH or active LOW, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active HIGH if $SL1_x$ is a "0" and active LOW if $SL1_x$ is a "1".

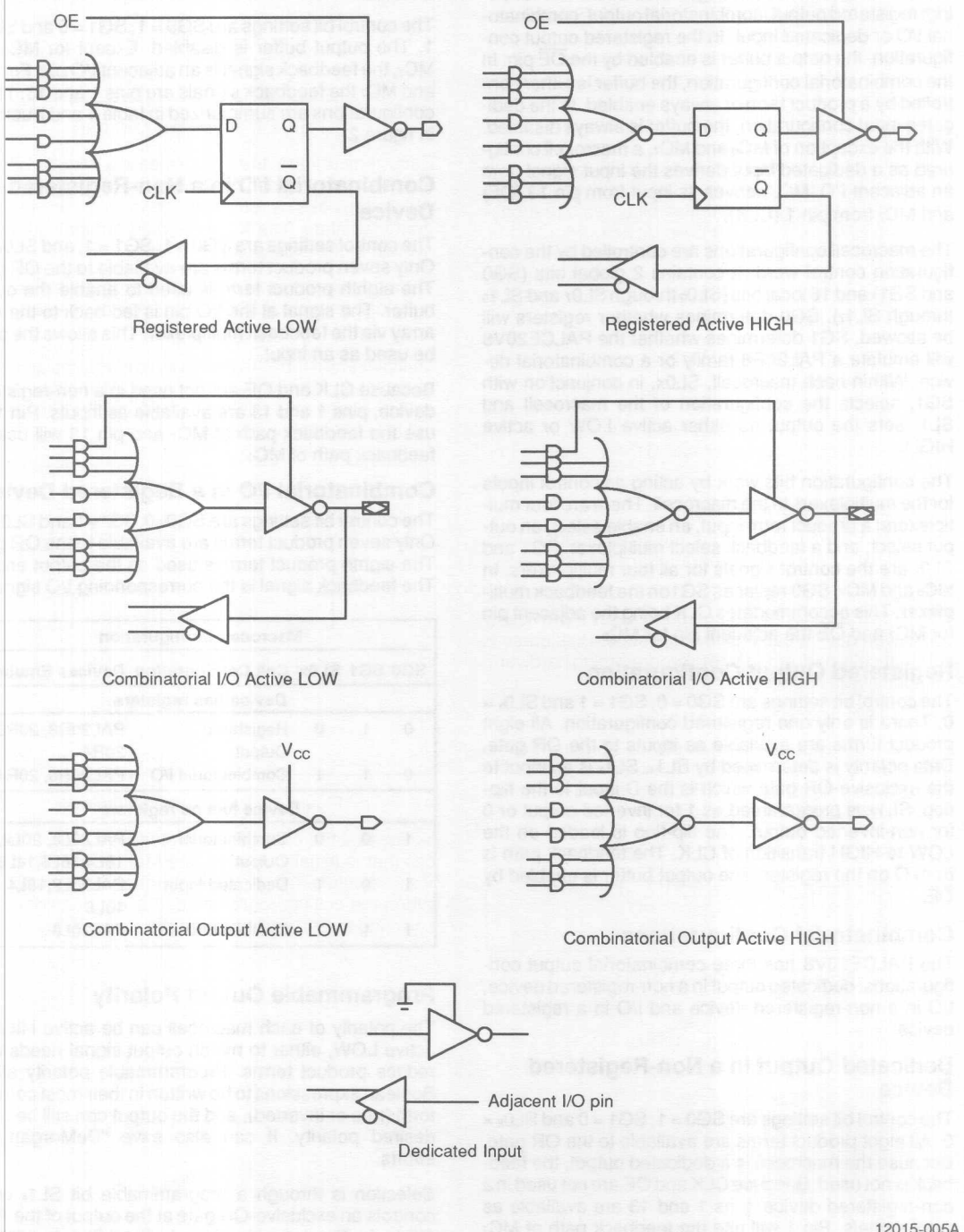


Figure 2. Macrocell Configurations

Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE20V8 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

Security Bit

A security bit is provided on the PALCE20V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during a bulk erase cycle.

Electronic Signature Word

An electronic signature word is provided in the PALCE20V8. It consists of 64 bits of programmable memory that can contain any user-defined data. The signature data is always available to the user independent of the security bit.

Programming and Erasing

The PALCE20V8 can be programmed on standard logic programmers. Approved programmers are listed in this data sheet.

The PALCE20V8 may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

Basic PAL Device Notation

The multi-input gates in the PAL device's programmable AND gate array are simplified in the logic diagrams. The PAL device notation for an AND gate, called a "product term" in a PAL device, is shown below.

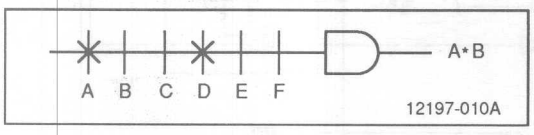


Figure 3. PAL Device AND Gate

This is equivalent to the standard logic notation below.

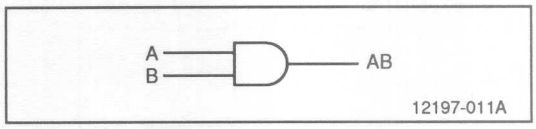


Figure 4. Standard AND Gate

Each vertical line in the PAL device is a potential input to the AND gate. At each crosspoint is a programmable bit, which provides a potential connection in the programmed state. The Xs in the diagram indicate a connection at the crosspoint.

In electrically erasable devices the crosspoints are originally disconnected. They are either connected or left open during device programming.

Multiplexers in the PAL device logic diagrams use a simple notation for maximum clarity. A 2:1 multiplexer that selects X when the control is LOW and Y when the control is HIGH is shown below.

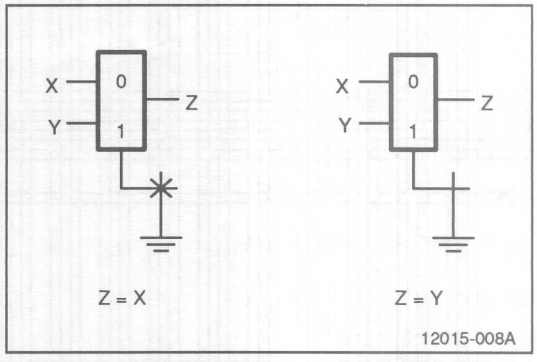


Figure 5. PAL Device Multiplexer

Notice that the control is operated by a programmable cell that is initially disconnected from GND, floating to V_{CC}, selecting the "1" path through the multiplexer. When the cell is programmed, it is connected to GND selecting the "0" path through the multiplexer.

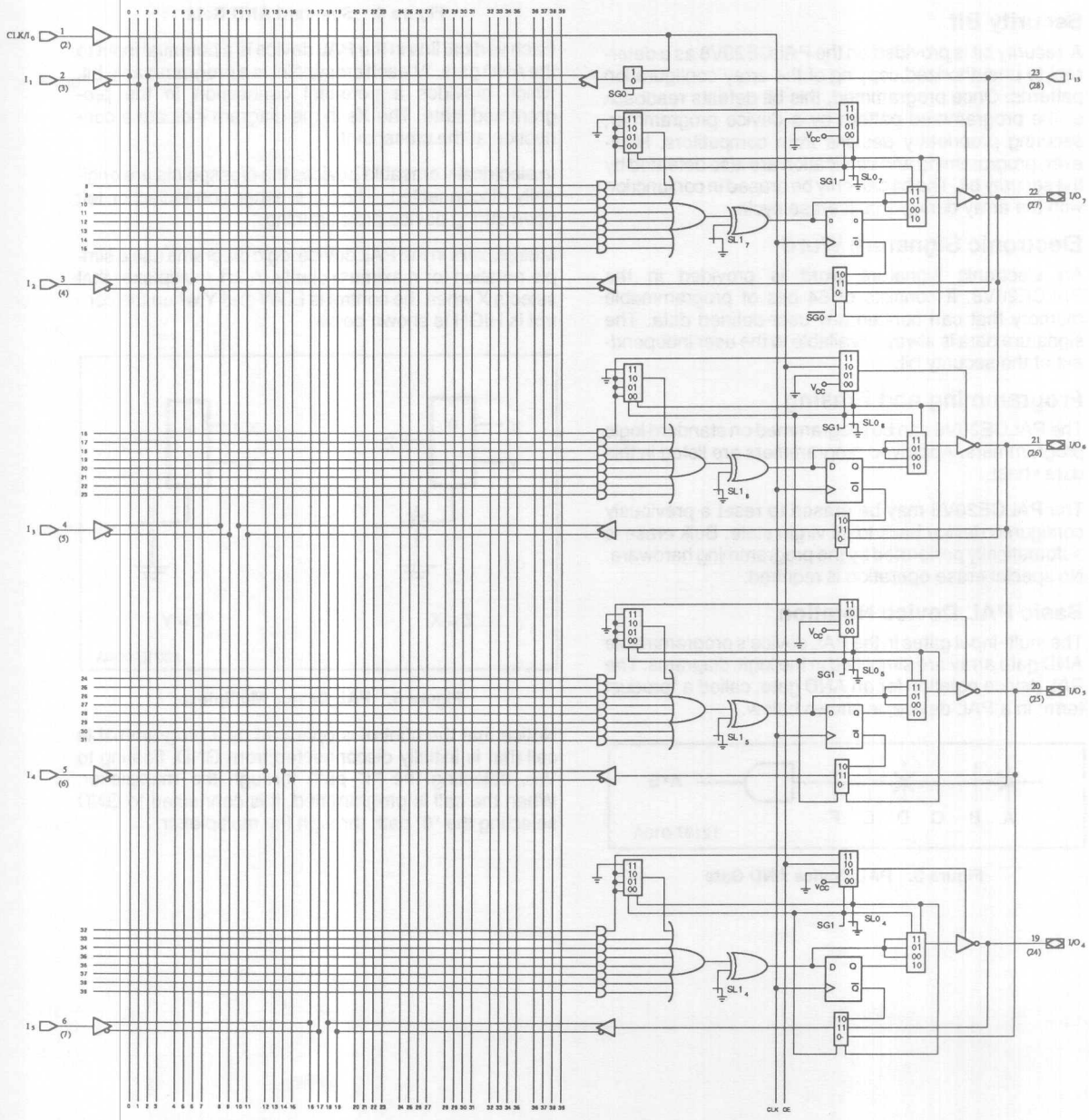


Figure 6. PALCE20V8 Logic Diagram

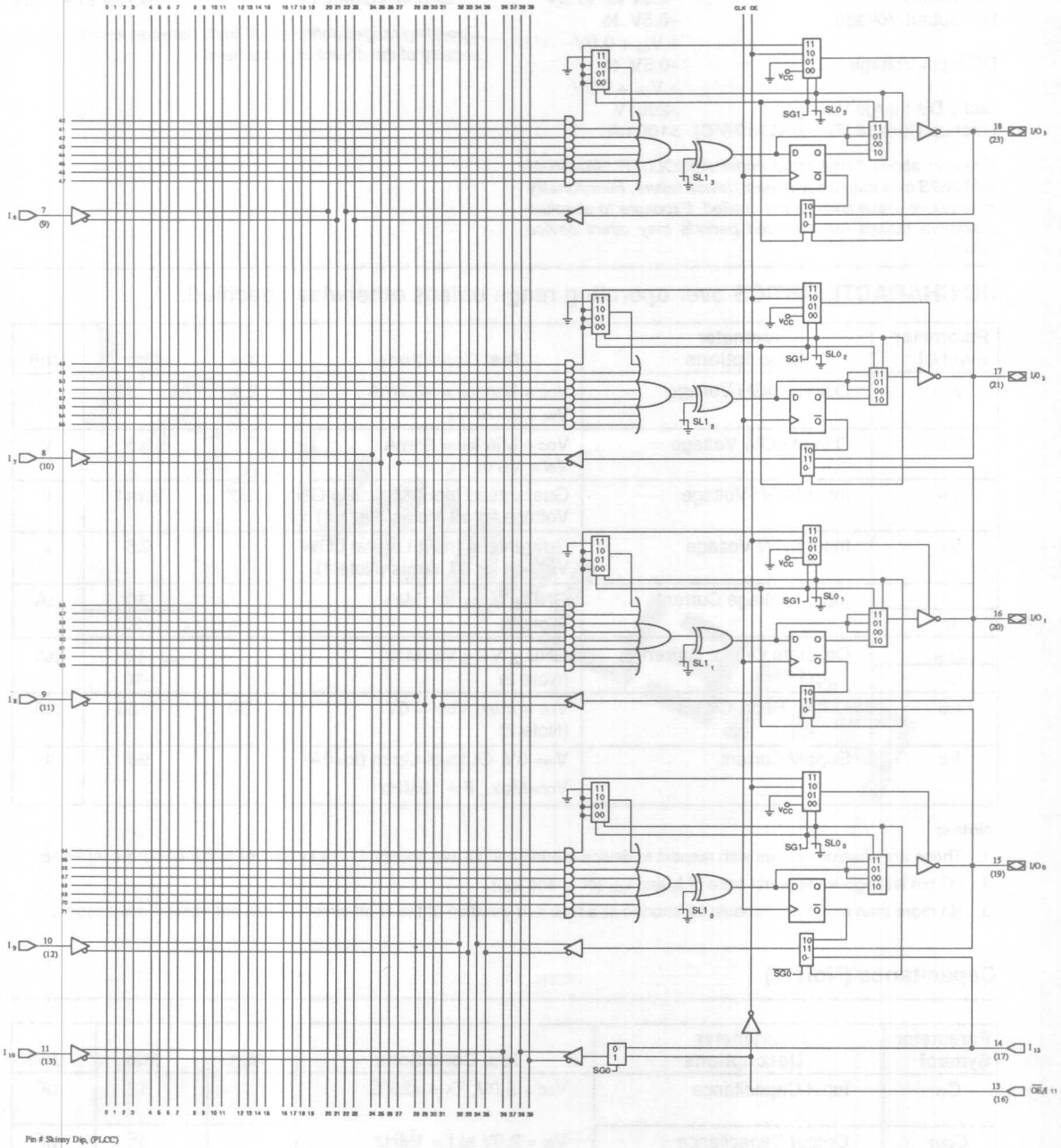


Figure 6. PALCE20V8 Logic Diagram (Continued)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature under bias	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5V to +7.0V
DC Output Voltage	–0.5V to + V_{CC} + 0.5V
DC Input Voltage	–0.5V to + V_{CC} + 0.5V
Static Discharge Voltage	>2001V
Latchup Current (T_A = 0°C to 75°C)	>100mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A) Operating Free Air	0°C to +75°C
Supply Voltage (V_{CC})	+4.75V to +5.25V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified.

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min I_{OH} = –3.2mA V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min I_{OH} = 24mA V_{IN} = V_{IH} or V_{IL}		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0	V_{CC}+1	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC} Max. (Note 2)		10	µA
I_{IL}				–10	
I_{OZH}	Off-State Output Current	GND ≤ V_{IN} ≤ V_{CC} Max. (Note 2)		10	µA
I_{OZL}				–10	
I_{OS}	Output Short-Circuit	V_{CC} = Max. V_{OUT} = 0V (Note 2)	–30	–130	mA
I_{CC}	Supply Current	V_{IN}= 0V, Outputs Open (I_O=0A) V_{CC}=Max., F = 15MHz		90	mA

PRELIMINARY

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. No more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Capacitance (Note 1)

Parameter Symbol	Parameter Descriptions	Test Conditions	Min.	Max.	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.0V, T_A = +25°C		12	pF
C_{OUT}	Output Capacitance	V_{IN} = 2.0V at f = 1MHz		15	pF

Note:

1. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where capacitance may be affected.

Switching Characteristics Over Commercial Operating Ranges (Note 1)

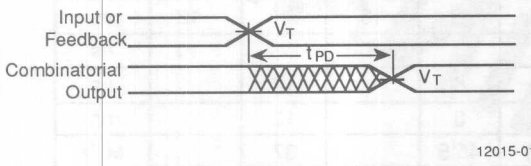
Parameter Symbol	Parameter Description		–15 Min.	–15 Max.	–25 Min.	–25 Max.	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 2)			15		25	ns
t_S	Setup Time from Input or Feedback to Clock		12		15		ns
t_H	Hold Time		0		0		ns
t_{CO}	Clock to Output			10		12	ns
t_{CF}	Clock to Feedback			8		10	ns
t_{WL}	Width of Clock	LOW	8		12		ns
t_{WH}		HIGH	8		12		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback $1/(t_S+t_{CO})$	45.5		37		MHz
		Internal Feedback $1/(t_S+t_{CF})$	50.0		40		MHz
		No Feedback $1/(t_{WH}+t_{WL})$	62.5		40		MHz
t_{PZX}	$\overline{OE}$ to Output Enable (Note 4)			15		20	ns
t_{PXZ}	$\overline{OE}$ to Output Disable (Note 4)			15		20	ns
t_{EA}	Input to Output Enable (Notes 4 and 5)			15		25	ns
t_{ER}	Input to Output Disable (Notes 4 and 5)			15		25	ns

PRELIMINARY

Notes:

1. Commercial Test Conditions: $R_1 = 200\Omega$, $R_2 = 390\Omega$ (see switching test circuit).
2. t_{PD} is tested with S_1 closed and $C_L = 50pF$ (including jig capacitance). $V_{IH} = 3V$, $V_{IL} = 0V$, $V_{OH} = V_OL = 1.5V$.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
4. For three-state outputs, enable times are tested with $C_L = 50pF$ to the 1.5V level; S_1 is open for high-impedance to HIGH tests and closed for high-impedance to LOW tests. Output disable times are tested with $C_L = 5pF$. HIGH to high-impedance tests are made to an output voltage of $V_{OH} - 0.5V$ with S_1 open; LOW to high-impedance tests are made to the V_{OL} to +0.5V level with S_1 closed.
5. Equivalent function to t_{PZX}, t_{PXZ} but using product term control.

SWITCHING WAVEFORMS



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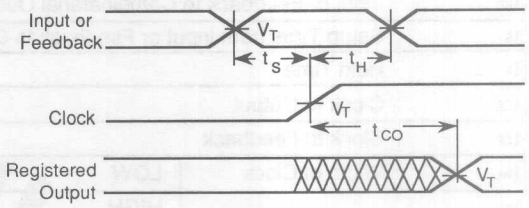
Combinatorial Output



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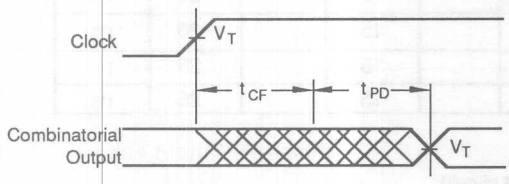
Registered Output



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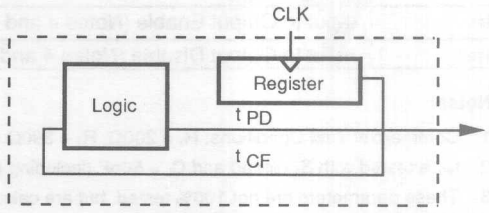
Clock to Feedback to Combinatorial Output (See Path at Right)



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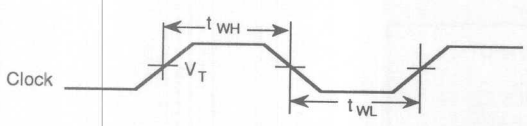

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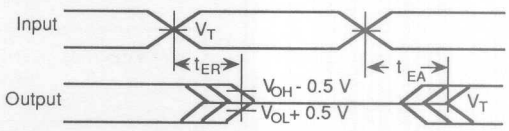
Clock Width



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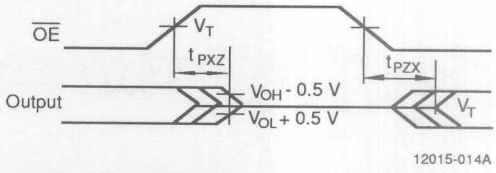
Input to Output Disable/Enable

Notes:

1. V_T = 1.5V
2. Input pulse amplitude 0V to 3.0V
3. Input rise time and fall times 2 – 5 ns typical



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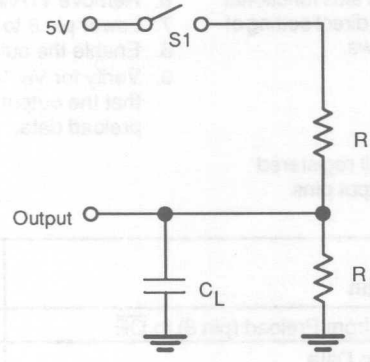
$\overline{OE}$ to Output Disable/Enable

SWITCHING TEST CIRCUIT



Switching Test Circuit

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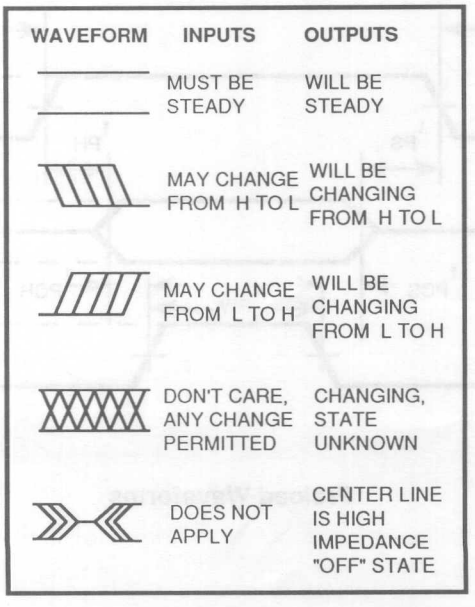
Notes on Testing Information

Specification	Switch S_1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5V
t_{PZX}, t_{EA}	Z → H: Open Z → L: Closed	50 pF	200 Ω	390 Ω	1.5V
t_{PXZ}, t_{ER}	H → Z: Open L → Z: Closed	5 pF	200 Ω	390 Ω	H → Z: V_{OH} –0.5V L → Z: V_{OL} +0.5V

Key to Switching Waveforms



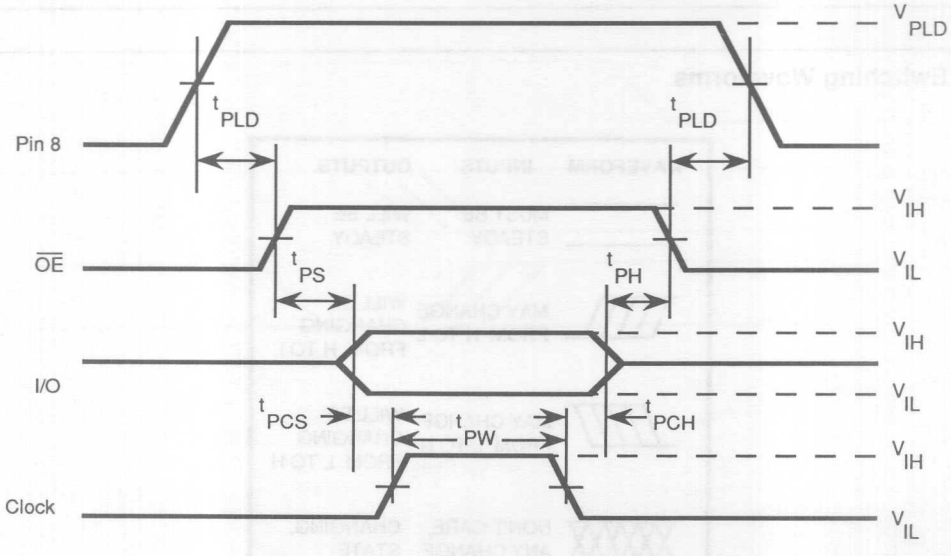
12015-018A

Output Register Preload

The PRELOAD function allows the registers to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure is as follows.

1. Raise V_{CC} to 5.0 V + 0.5 V.
2. Set pin 8 to 13.5 V ± 0.5 V.
3. Set $\overline{OE}$ HIGH.
4. Apply the desired value (V_{IL}/V_{IH}) to all registered output pins. Leave combinatorial output pins floating.
5. Clock pin 1 from V_{IL} to V_{IH}.
6. Remove V_{IL}/V_{IH} from all registered outputs.
7. Lower pin 8 to V_{IL}/V_{IH}.
8. Enable the output registers by lowering $\overline{OE}$.
9. Verify for V_{OL}/V_{OH} at all registered output pins. Note that the output pin signal will be the inverse of the preload data.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_{PLD}	Setup and Hold Time from Preload (pin 8) to $\overline{OE}$	50	50		µs
t_{PS}	Setup Time from $\overline{OE}$ to Data	1	1		µs
t_{PH}	Hold Time from Data to $\overline{OE}$	1	1		µs
t_{PCS}	Setup Time from Data to Clock	1	1		µs
t_{PCH}	Hold Time from Clock to Data	1	1		µs
dV_r/dt	V_{PLD} Rising Slew Rate (pin 8)	10		100	V/µs
dV_f/dt	V_{PLD} Falling Slew Rate (pin 8)		2	3	V/µs



12197-008A

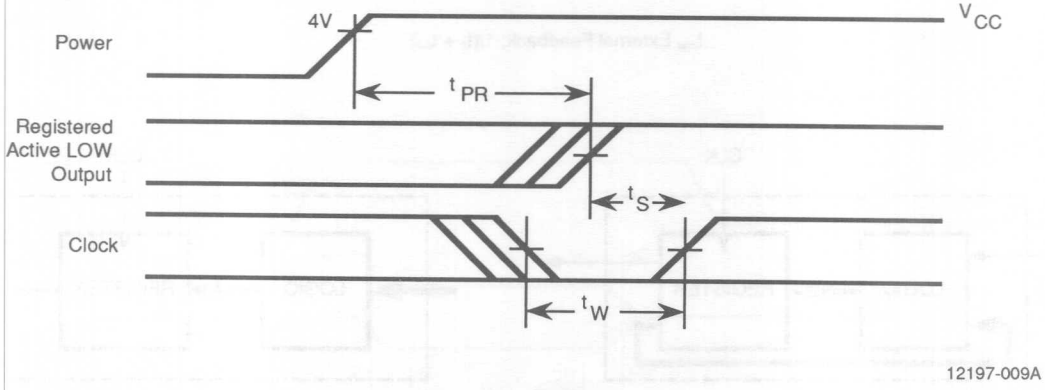
Preload Waveforms

Power-Up Reset

The PALCE20V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Descriptions	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		100	µs
ts	Input or Feedback Setup Time	See Switching Characteristics		
tw	Clock width			



Power Up Reset

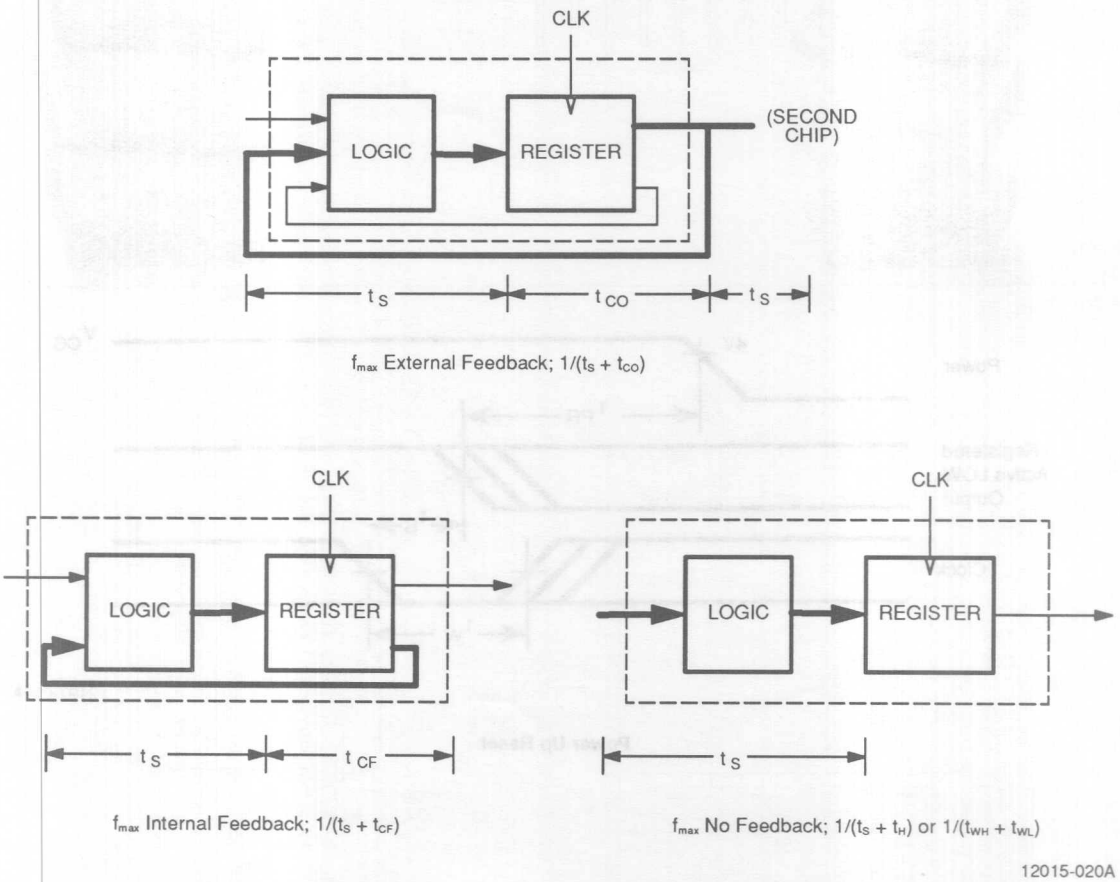
f_{MAX} Parameters

The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for three types of synchronous designs.

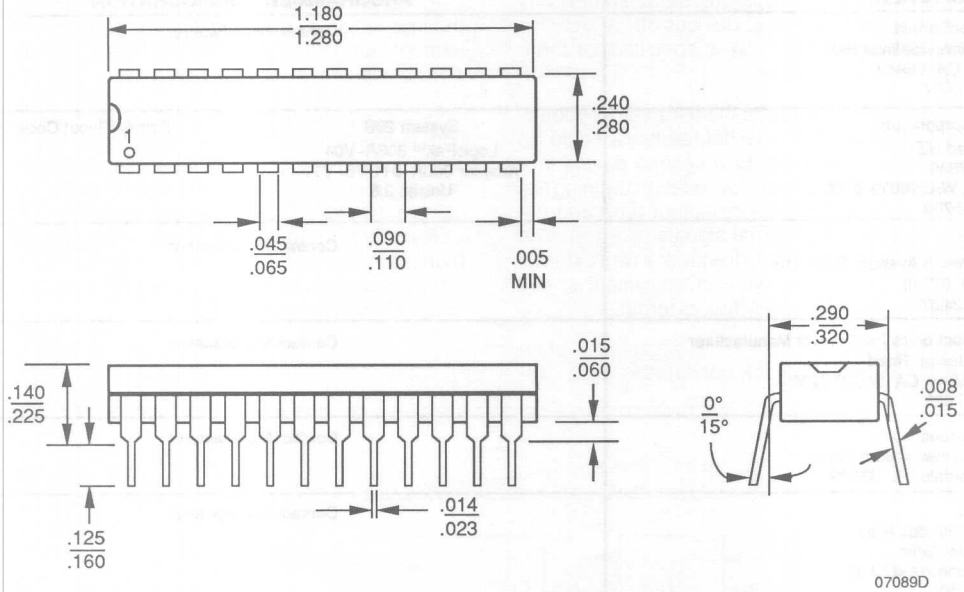
The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop outputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_S$). This f_{MAX} is designated "f_{MAX} internal".

The third type of design is a simple data path application. In this case, input data is presented to the flip-flop and clocked through; no feedback is employed. Under these conditions, the period is limited by the sum of the data setup time and the data hold time ($t_S + t_H$). However, as lower limit for the period of each f_{MAX} type is the minimum clock period ($t_{WH} + t_{WL}$). Usually, this minimum clock period designates the period for the third f_{MAX}, designated "f_{MAX} no feedback)."



PHYSICAL DIMENSIONS
PD 3024



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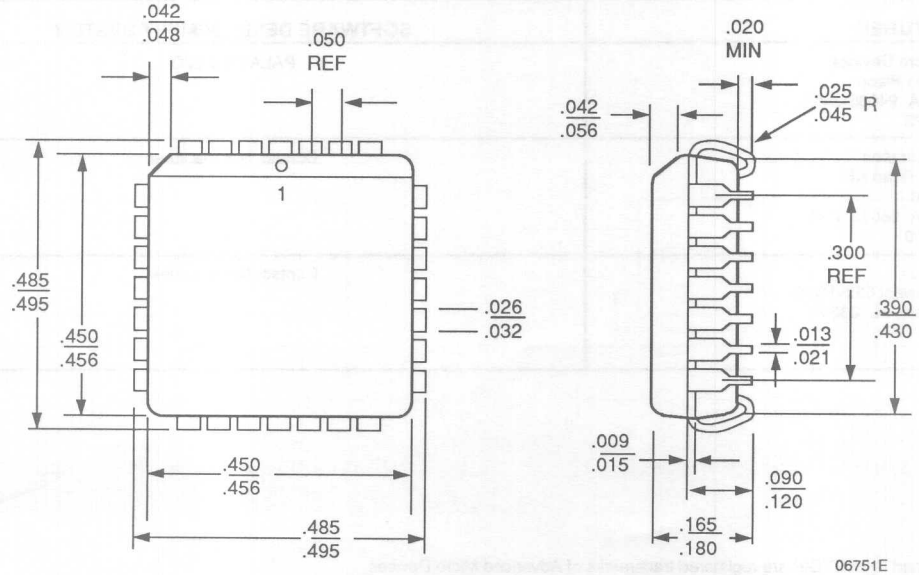

06751E

Programmers/Development Systems (Subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION
Adams MacDonald 2999 Monterey/Salinas Hwy. Monterey, CA 93940 (408) 373-3607	Contact Manufacturer
Data I/O Corporation Willow Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	System 29B Family/Pinout Code LogicPak™ 303A–V04 Adapter 303A–011A/B–V11 Unisite 2.6
Digelec Inc. 1602 Lawrence Avenue, Suite 113 Ocean, NJ 07712 (201) 493-2420	Contact Manufacturer
Kontron Electronics Inc.Contact Manufacturer 1230 Charleston Road Mountain View, CA 94039-7230 (415) 965-7020	Contact Manufacturer
Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309	Contact Manufacturer
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact Manufacturer
Stag Microsystems Inc. 1600 Wyatt Drive, Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact Manufacturer
Varix Corporation 1210 E. Campbell Road, Suite 100 Richardson, TX 75081 (214) 437-0777	Contact Manufacturer
MANUFACTURER	**SOFTWARE DEVELOPMENT SYSTEM**
Advanced Micro Devices 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM 2.23D
Data I/O Corporation 10525 Willow Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	Contact Manufacturer
Logical Devices 1201 E. Northwest 65th Place Fort Lauderdale, FL 33309	Contact Manufacturer

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